GLOBAL RESEARCH IMMERSION PROGRAM FOR YOUNG SCIENTISTS

Design of a Hybrid Brain-Inspired Chip Targeting Artificial General Intelligence

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Abstract: A **hybrid brain-inspired computing chip** is designed which is compatible with multiple neural network models. The chip contains multiple functional cores, enabling support for **vast and complex neural networks of a variety of models**. It is supposed to reduce the **deployment cost** of neuromorphic neural network models, optimize **computational and power efficiency**, and promote the development of **artificial general intelligence (AGI).**

Keywords: artificial general intelligence, brain-inspired chip, neuromorphic neural network

Background: Previous neural networks with single model remains difficult to handle difficult dynamic problems. A better solution requires the achievement of AGI, which requires the implementation of various neural network models. To provide a general platform for AGI, we want to develop a hybrid brain-inspired chip that should be capable of both artificial neural networks (ANNs) and neuromorphic neural networks such as spike neural networks (SNNs).

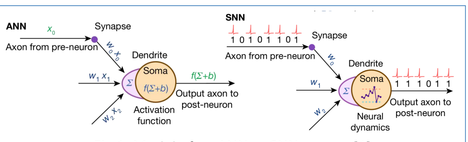

Fig 1: Model of an ANN or SNN neuron [1]

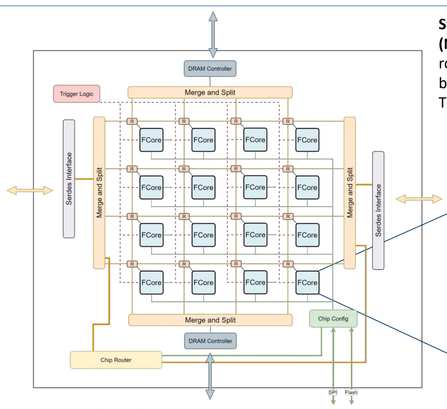

Fig 2: Top-level architecture of the chip

Structure: The chip applicates a **2D mesh many-core array** and **Network on Chip (NoC) architecture**. Multiple functional cores are implemented and an inter-core router is used for data transfer. Inside a functional core, both ANNs and SNNs can be achieved through a shared computing path using the dendrite and soma unit. Thus, the chip can run a specific neural network according to configuration.

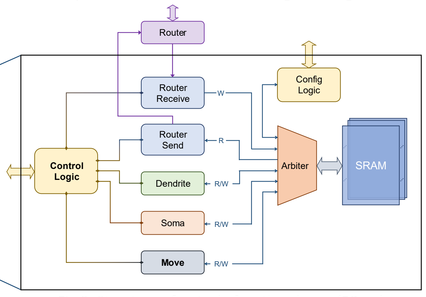

Fig 3: Structure of a single functional core (FCore)

My main task in the project is the design and validation of two functional core units: the **move unit** and the **control unit**. The move unit targets at the merge and split of vectors in the memory space, achieved by writing data to specified address. The control unit is responsible for reading primitives and sending them to corresponding execution units in a certain order.

Move Unit

Merge and split functions are realized separately in the move unit. The unit does not add or minus two vectors according to the literal meaning, but carry data of the vectors to specified address. The processing of these vectors are realized by other units.

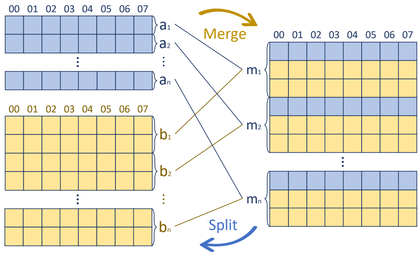

Fig 4: Merge and split logic

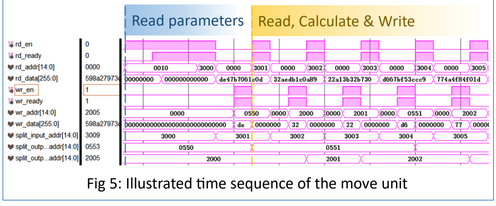

Fig 5: Illustrated time sequence of the move unit

Control Unit

Two control modes are developed for different occasions. **The simple mode** does not consider the dependency of primitives, and executes the commands one by one. **The normal mode** uses a dependency queue to achieve a pipeline effect, and multiple primitives can be executed at the same time to improve computing efficiency.

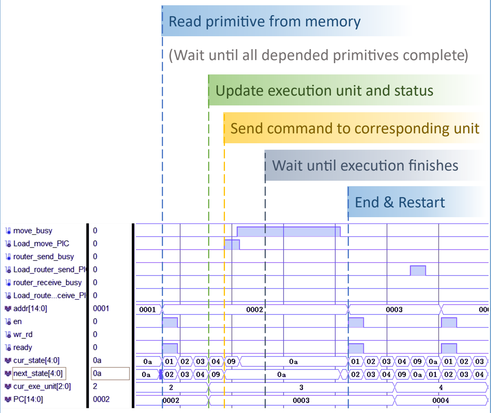

Fig 6: Illustrated time sequence of the control unit

References:
[1] Pei J, Deng L, Song S, et al. Towards artificial general intelligence with hybrid Tianjic chip architecture[J]. *Nature*, 2019, 572(7767): 106-111.
[2] Akopyan F, Sawada J, Cassidy A, et al.Truenorth: Design and tool flow of a 65 mw 1 million neuron programmable neurosynaptic chip[J]. *IEEE transactions on computer-aided design of integrated circuits and systems*,2015, 34(10): 1537-1557.